REMARKS

Claims 16-33 are pending in the present application. Claims 1-15 were previously cancelled. Claims 29-33 were previously withdrawn. No new matter has been added. Applicants respectfully request reconsideration of the claims in view of the following remarks.

The amendments filed December 22, 2006 and April 24, 2007 were objected to under 35 U.S.C. 132(a) because they introduce new matter into the disclosure. It is alleged that the added material not supported by the original disclosure as follows: In paragraph [0025], as amended on December 22, 2006, the amendment "such that the notched spacer is thinner along the surface of the substrate, as illustrated in FIG. [1]j," is a new matter.

The Examiner makes it clear that objection is due to the reference to Figure 1j. Figure 1j is discussed below.

The drawings are objected to, because it is alleged that amended Figure 1j, filed on June 24, 2008 introduces new matter. The Examiner states:

> Figure 1j is objected to, because figure 1j does not depict a notched spacer is thinner along the surface of the substrate, as recited in original claim 16. Figure 1j depicts a notched spacer alongside the gate electrode, such that the notched spacer is thinner at a first portion closer to the surface of the substrate than at a second portion being further from the substrate. Note that the phrase "a notched spacer is thinner along the surface of the substrate" is not synonymous to the phrase " a notched spacer is thinner at a first portion closer to the surface of the substrate than at a second portion being further from the substrate.

Office Action dated December 3, 2008, Pages 12 and 13.

Applicants disagree, the phrase "a notched spacer is thinner at a first portion closer to the surface of the substrate than at a second portion being further from the substrate" *is* synonymous with "a notched spacer is thinner along the surface of the substrate." Figure 1j illustrates both phrases.

Figure 1j was added as a new figure in a previous amendment to overcome Examiner's 112 rejection. Figure 1j was added to further prosecution and has support in the specification and the claims. Figure 1j shows a notched spacer alongside the gate electrode, such that the notched spacer is thinner along the surface of the substrate. Therefore, Figure 1j is supported by original claim 16 and paragraph [0025], as well as original paragraph [0010].

Applicants respectfully request reconsideration of the objection to Figure 1j and the objection to the specification referring to Figure 1j.

Claims 16-28 were rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. It is alleged by the Examiner that the claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicants disagree, paragraph [0010] states in part, "The notched spacer is formed alongside the gate electrode such that a portion of the notched spacer is completely, or partially removed along the corner formed between the surface of the substrate and the gate electrode sidewall." Clearly, a notched spacer partially removed along the corner formed between the surface of the substrate and the gate electrode is "thinner along the surface of the substrate." Removing any portion of the described corner must make the notch thinner. Partially removing a portion of the described corner obviously means that there is a portion left however; it follows that since there is a portion removed, the notch must be thinner.

The Examiner states:

> The recitation of "a portion of the notched spacer is completely or partially removed along the corner formed between the surface of the substrate and the gate electrode sidewall" does not necessarily mean that the notched spacer is thinner along the surface of the substrate. Partially removing a portion of the notched spacer along the corner formed between the surface of the substrate and the gate electrode sidewall, can mean that an entire small portion of spacer is removed along the corner, thus leaving another portion of the spacer, which is not covered by the mask, intact. There is certainly no support for the top of the thinner spacer being aligned with the bottom of the mask, as depicted in figure 1j.

Office Action dated December 3, 2008, Pages 13 and 14.

The Examiner seems to be describing a further embodiment of the present invention. There is no limitation in the claim language concerning the alignment of the notch nor the notch height. While those of ordinary skill in the art would find the Examiner's embodiment some what unlikely, it is a welcome embodiment covered at least by claim 16. The embodiment shown in Figure 1j is a more likely embodiment. Moreover, many more such embodiments may be drawn depicting the various thicknesses and notch heights produced by various etch processes.

During patent examination, the pending claims must be "given their broadest reasonable interpretation consistent with the specification." The Federal Circuit's *en banc* decision in *Phillips v. AWH Corp.*, 415 F.3d 1303, 75 USPQ2d 1321 (Fed. Cir. 2005), expressly recognized that the USPTO employs the "broadest reasonable interpretation" standard:

> The Patent and Trademark Office ("PTO") determines the scope of claims in patent applications not solely on the basis of the claim language, but upon giving claims their broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364[, 70 USPQ2d 1827] (Fed. Cir. 2004).

MPEP 2111.

To those of ordinary skill in the art, it is obvious that a notched area is a thinner area. The ordinary and plain meaning of the word "notched" means an indentation, not a protrusion.

Paragraph [0025] and Figures 1D and 1E are reproduced below.

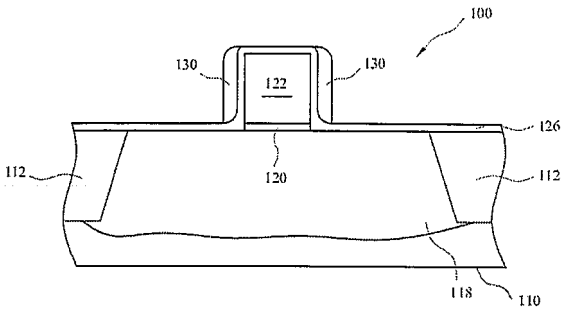


FIG. 1D

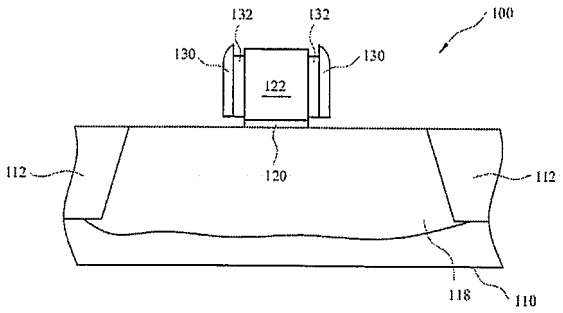


FIG. 1E

Originally filed Figures 1D and IE.

As illustrated in FIG. 1e, the portion of the first dielectric layer 126 (FIG.1d) located under the notched-spacer masks 130 is removed due to the isotropic etching process, thereby creating a notched spacer. The width of the notch will be dependent upon the thickness of the first dielectric layer 126 and the notch height may be controlled by varying the etch duration. Furthermore, FIG. 1e illustrates the situation in which the first dielectric layer 126 is removed completely to the gate electrode 122. In other situations, a portion of the first dielectric layer 126 may remain on the side of the gate electrode 122. This may be desirable, for example, when it is preferred to control the depth and angle of the implant or to protect the gate electrode 122 or gate dielectric 120 from damage during the etching process or other processes.

Originally filed paragraph [0025]. (Emphasis added.)

The Examiner states, "The recitation i[n] paragraph [0025] does not clarify from which element the notched spacer alongside the gate electrode is thinner than." Applicants disagree.

Paragraph [0025] states, "the portion of the first dielectric layer 126 located under the notched-spacer masks 130 is removed due to the isotropic etching process, thereby creating a notched spacer." Making it clear that the notch is located under the notched-spacer masks 130. It is obvious that the remainder of the paragraph speaks to the thickness, thinness, and height of the notch as compared to the "non-notched" portion of the notched spacer. Further, amended claim 16 states, "forming a notched spacer alongside the gate electrode such that a thickness of

the notched spacer alongside the gate electrode is thinner near the substrate..." making it clear that the thickness comparison is between the notched and the non-notched areas of the notched spacer.

In the final Office Action dated December 3, 2008, the Examiner states, "Applicant further argues that the recitation of "the notch height may be controlled by varying the etch duration." means to one of ordinary skill in the art, that "it is the thinness of the notched spacer alongside the gate electrode near the substrate that is controlled by varying the etch duration."""

While not stated in precisely that manner, and supported by additional sections of the specification and claims, it is the case that the notch height may be controlled by the same etch process as the thinness of the notched spacer. As paragraph [0025] states, "the notch height may be controlled by varying the etch duration." The layer 126 (for example SiO_2) alongside the gate electrode near the substrate is not protected by a mask; therefore, it is easily recognized, by one of ordinary skill in the art, that the thinness of the notched spacer alongside the gate electrode near the substrate is controlled by varying the etch duration.

Those of ordinary skill in the art will further understand that the portion of the first dielectric layer 126 (the notch height), located under the notched-spacer masks 130 may remain on the side of the gate electrode 122. An isotropic etch tends to clear the thickest portion of a dielectric layer last. Thus, it follows that an etch of relatively short duration may leave a portion of dielectric layer 126 on the lower portion of the side of the gate electrode 122, and an etch of relatively long duration may leave substantially no portion of layer 126 alongside the gate electrode near the substrate. An etch of even longer duration may leave substantially no portion of layer 126 alongside the gate electrode near the substrate, and due to the isometric properties of the etch, further etch layer 126 behind the notched spacer masks 130 raising the notch height.

Therefore, within the specification as originally filed is the description of a method to control the thickness of the notch alongside the gate electrode near the substrate. The Examiner's allegation that the claim element "a thickness of the notched spacer alongside the gate electrode is thinner near the substrate," is not taught in the specification is incorrect.

Moreover, it is clear to one of ordinary skill in the art that: 1) the spacer is alongside the gate electrode; 2) the area of the spacer that is unprotected by the mask is the area of the spacer that is etched; and 3) the area of the spacer that is unprotected by the mask is along the surface of the substrate. Therefore, to one of ordinary skill in the art, thinner along the surface of the substrate does indeed state that the notched spacer is thinner alongside the gate electrode near the substrate. Amended claim 16, reciting, "forming a notched spacer alongside the gate electrode such that a thickness of the notched spacer alongside the gate electrode is thinner near the substrate," is supported at least by original paragraphs [0010] and [0025].

Further, even if the Examiner finds that claim 16 is not sufficiently supported in the original specification, MPEP 608.01(l) states, "In establishing a disclosure, applicant may rely not only on the description and drawing as filed, but also on the original claims if their content justifies it." Claim 16, as originally filed, recites in part, "forming a notched spacer alongside the gate electrode such that the notched spacer is thinner along the surface of the substrate ...", and accordingly, provides the necessary support for amended claim 16 which states, "forming a notched spacer alongside the gate electrode such that a thickness of the notched spacer alongside the gate electrode is thinner near the substrate..."

Thus, amended claim 16, and dependant claims 17-23 are supported by the original specification in paragraphs [0010], [0025] and Figures 1D and 1E. Applicants respectfully submit that the rejection of claim 16 is thus traversed. Since claims 17-23 depend from claim 16,

the same arguments as the independent claim 16 apply to these dependent claims. Therefore, the rejection of claims 17-23 has been traversed.

Claims 16-23 were rejected under 35 U.S.C. 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 16, the Examiner states, "a thickness of the notched spacer alongside the gate electrode is thinner near the substrate, as recited in claim 16, are unclear from which element the notched spacer alongside the gate electrode is thinner than." As original claim 16 stated and as paragraph [0025] clarifies, "the notched spacer is thinner along the surface of the substrate." The notch is thinner than the non-notch part of the spacer. That is the plain meaning of notch.

Claims 16 and 23 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No.7,009,264 to Schuegraf, *et al.* (hereinafter "Schuegraf") in view of U.S. Patent No. 5,215,936 to Kinugawa, *et al.* (hereinafter "Kinugawa"). Applicants respectfully traverse this rejection.

The Examiner states, "Schuegraf et al. do not teach performing a first ion implant wherein only the gate electrode and the notched spacer act as masks during the first ion implant, the first ion implant using ions of the first conductivity type." The Examiner continues by stating, "Kinugawa teaches in figure 3C and related text performing a first ion implant wherein only the gate electrode 15 and the spacer 17A act as masks during the first ion implant, the first ion implant using ions of the first conductivity type N in a region 11 in the substrate having a

first conductivity type N." Applicants disagree. Claim 16 states "forming a gate electrode on a region in a substrate, the region in the substrate having a first conductivity type."

Kinugawa does not teach performing a first ion implant using ions of the first conductivity type, wherein only the gate electrode and the spacer act as masks, as seen from the text quoted from Kinugawa below.

> A step of ion-implanting an impurity into the semiconductor body with the gate electrode as a mask, followed by a thermal treatment to form first and second impurity regions of the opposite conductivity type in surface portions of the semiconductor body, a step of forming an insulating member on the first and second impurity regions so as to be in contact with at least the side wall of the gate electrode, and a step of ion implanting an impurity of the opposite conductivity type into the first and second impurity regions with said first gate and insulating member as a mask.

Kinugawa, Column 2, lines 57-68.

Kinugawa above describes implanting an n- region into a p-type surface portion of the semiconductor body (a p-well structure), forming sidewalls, and then implanting an n+ region into the p-well structure. In contrast, claim 16 requires "performing a first ion implant ... using ions of the first conductivity type," where the substrate has a first conductivity type. Thus, according to the present specification, an N-channel device receives a p-type implant, because the substrate of an N-channel device is p-type and a P-channel device receives an n-type implant, because the substrate of a P-channel device is n-type. Therefore, Kinugawa does not teach performing a first ion implant ... using ions of the first conductivity type. Thus, neither Schuegraf nor Kinugawa, either alone or in combination, teaches all of the limitations of claim 16. Moreover, even if the references could be properly combined, the combination of the

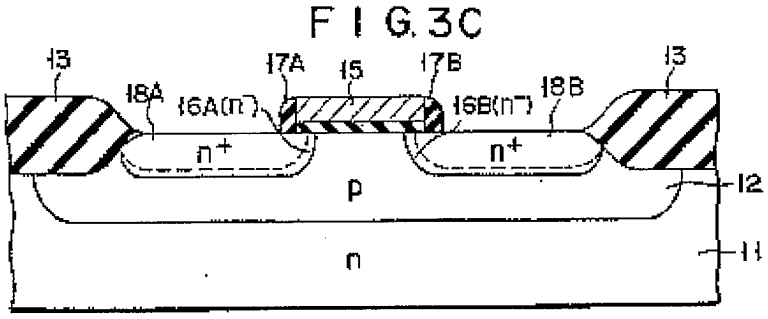
references would not form the presently claimed invention. The rejection to claim 23 is overcome at least due to the dependency of claim 23 on claim 16.

In response the Examiner states:

> It is not understood from applicant's argument why Kinugawa's recitation of "implanting an n-region into a p type surface portion of the semiconductor body (a p-well structure), forming sidewalls, and then implanting an n+ region into the p-well structure", does not read on the claimed limitation of "performing a first ion implant... using ions of the first conductivity type, where the substrate has a first conductivity type". Kinugawa performs a first ion implant (of n+ region) using ions of the first conductivity type N, where the substrate 11 has a first conductivity type N.

Office Action dated December 3, 2008, Page 15.

The Examiner appears to be arguing that Kinugawa is implanting the n regions in the substrate 11, which is clearly not the case, as seen in Kinugawa Figure 3C; or that a p-well has a conductivity type N. Neither supposition is supported by Kinugawa.



Kinugawa Figure 3C.

As seen from Figure 3C, the implant does not reach the n layer 11 and the implanted area 12 is p-type.

Claims 17 and 18 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Schuegraf and Kinugawa, as applied to claim 16 above, and further in view of U.S. Patent No. 6,610,571 to Chen, *et al.* (hereinafter "Chen"). Applicants respectfully traverse these rejections.

Claims 17 and 18 were rejected under 35 U.S. C. § 103(a) as assertedly being unpatentable over Schuegraf and Kinugawa as applied to claim 16 above, and further in view of Chen, *et al.* (U.S. Patent No. 6,610,571, hereinafter "Chen"). Applicants respectfully traverse this rejection. Claims 17 and 18 are dependent on claim 16, thus, by at least the reason of their dependency, the rejection of claims 17 and 18 is traversed.

Claims 16 and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,417,084 to Singh, *et al.* (hereinafter "Singh") in view of Kinugawa. Applicants respectfully traverse these rejections.

The Examiner concedes that, "Singh et al. do not teach performing a first ion implant wherein only the gate electrode and the notched spacer act as masks during the first ion implant, the first ion implants using ions of a second conductivity type." Rather, once again, the Examiner points to Kinugawa. As discussed above, Kinugawa does not teach the implant limitations as claimed. Therefore, neither Singh nor Kinugawa teaches all of the limitations found in claim 16; therefore, the rejection of claim 16 has been traversed. The rejection of claim 22 at least by virtue of its dependency on claim 16 has also been traversed.

Claims 17 and 19 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over by Singh and Kinugawa, as applied to claim 16 above, and further in view of Chen. Applicants respectfully traverse this rejection. Claims 17 and 19 are dependent on claim 16, thus, by at least the reason of their dependency, the rejection of claims 17 and 19 is traversed.

Claims 20 and 21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Schuegraf and Kinugawa, or over Singh and Kinugawa, as applied to claim 16 above, and further in view of Applicant Admitted Prior Art (AAPA). Claims 20 and 21 are dependent on claim 16, thus, by at least the reason of their dependency, the rejection of claims 20 and 21 is traversed.

Claims 24, 27, and 28 were rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Kinugawa.

Chen specifically teaches away from claim 24. "Due to the loss of liner oxide in these regions 54, device isolation and device performance is negatively affected; this loss of liner oxide must therefore be avoided." (Chen, Column 4, lines 39-42). See Chen Figure 4 below.

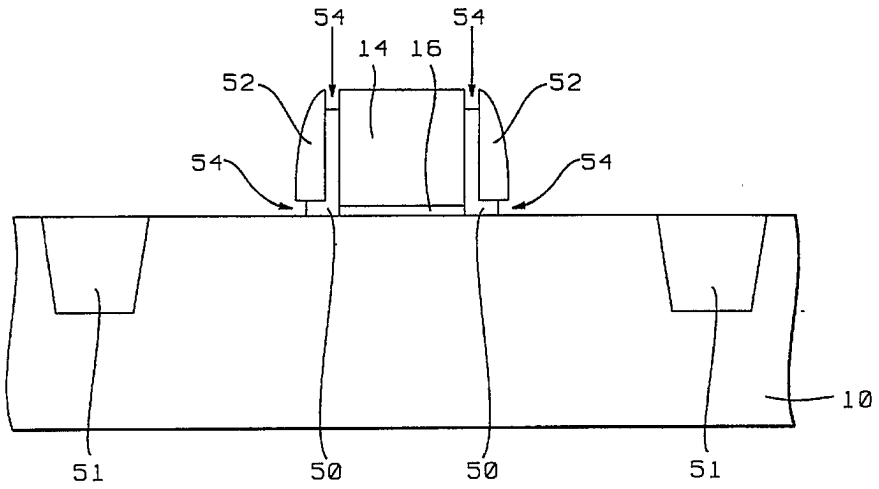


FIG. 4 – Prior Art

Chen, Figure 4.

As can be seen from Figure 4, it is regions 54 that Chen cautions against etching. The oxide liner is thereby formed into an L shape. This is the opposite of the notched spacer recited by Applicants' specification. Therefore, Chen teaches away, in fact cautions against, the modification proposed in the Office Action. A reference may be said to "teach away" from the

claimed invention when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the Applicants. This is clearly the case for Chen. Moreover, the short comings of Kinugawa have been discussed above and will not be discussed further here. Therefore, neither Chen nor Kinugawa teaches all of the claim limitations of claim 24. Further Chen teaches away from claim 24. Thus, the rejection of claim 24 has been overcome. Since claims 25-28 depend from claim 24, the rejection of claims 25-28 are overcome at least by their dependency on claim 24.

The Examiner responded to the above argument by stating:

> Even if Chen cautions against etching regions 54, the examiner does not suggest to modify the etching of regions 54. The Examiner suggests to modify Chen's device by using "a first ion implant is performed after the spacer mask has been removed...", as taught by Kinugawa. Therefore, it is unclear to the Examiner how Chen teaches away and cautions against, the above modification, as proposed in the Office Action. Furthermore, although the oxide liner is formed into an L shape, this is not the opposite of the notched spacer recited in the claims.

Office Action dated December 3, 2008, Page 16.

Claim 24 recites in part, "etching the first layer to form a notched spacer wherein the spacer mask acts as a mask, and wherein the etching removes at least a portion of the first layer along a surface of the substrate, thereby forming a notch in the notched spacer alongside the gate electrode near the substrate."

The ordinary meaning of a notch is an indention on an edge or surface. Chen does not teach forming a notch in the spacer; in fact, Chen teaches an L shaped protrusion. The shortcomings of Kinugawa were discussed above. Therefore, either alone or in combination, neither Chen nor Kinugawa teaches each and every limitation of claim 24.

Claims 25 and 26 were rejected under 35 U.S.C. § 103(a) as being unpatentable by Chen and Kinugawa, as applied to claim 24 above, and further in view of Applicant Admitted Prior Art (AAPA). Claims 25 and 26 depend from claim 24 and add further limitations. It is respectfully submitted that these dependent claims are allowable by reason of depending from an allowable claim as well as for adding new limitations.

The Examiner further argues that, "Figure 1f and related text describe performing a first ion implant wherein only the gate electrode and two notched spacers 132 act as masks. There is no support in figure 1f and related text for the claimed limitations of "performing a first ion implant wherein only the gate electrode and the notched spacer act as masks", as recited in claim 16 and as argues by applicant." Office Action dated December 3, 2008, Page 14.

Claim 16 recites in part, "the method comprising... forming a notched spacer alongside the gate electrode," therefore the claim's scope may include more than one notched spacer alongside the gate electrode.

In view of the above, Applicants respectfully submit that this response complies with 37 C.F.R. § 1.116. Applicants further submit that the claims are in condition for allowance. No new matter has been added by this amendment. If the Examiner should have any questions, please contact Mary Adams-Moe, Applicants' Attorney, at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, in the event that there are any fees due, please charge the same, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

March 3, 2009
Date

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